1. A semiconductor structure comprising:

a Schottky layer adapted to be etched at a first etch rate by an etchant; and

a contact layer disposed above the Schottky layer and adapted to be etched by the etchant at a second etch rate that is substantially faster than the first etch rate;

wherein the contact layer provides an opening through the contact layer exposing a region of a top surface of the Schottky layer, the region having a first width; and

wherein the region of the top surface of the Schottky layer provides a recess of a second width smaller than the first width.

2. The semiconductor recited in claim 1 wherein the Schottky layer contains Aluminum.

3. The semiconductor recited in claim 2 wherein the Schottky layer comprises at least about 35 percent Aluminum.

4. The semiconductor recited in claim 3 wherein the Schottky layer is $Al_{0.6}In_{0.4}As$.

5. The semiconductor recited in claim 1 wherein the contact layer comprises less than about ten percent Aluminum.

6. The semiconductor recited in claim 1 wherein the contact layer is substantially free of Aluminum.

7. A transistor structure comprising:

a Schottky layer adapted to be etched at a first etch

rate by an etchant; and

a contact layer disposed above the Schottky layer and adapted to be etched by the etchant at a second etch rate that is substantially faster than the first etch rate;

wherein a region above a portion of a top surface of the Schottky layer is substantially free of the contact layer, the portion having a first width;

wherein the portion of the top surface of the Schottky layer provides a recess of a second width smaller than the first width; and

wherein the recess of the second width is adapted to receive a gate electrode.

8. The transistor recited in claim 7 wherein the Schottky layer comprises at least about 35 percent Aluminum and the contact layer comprises less than about ten percent Aluminum.

9. A method of forming a semiconductor comprising:

forming a Schottky layer adapted to be etched by a first etchant at a first etch rate;

forming a contact layer above the Schottky layer adapted to be etched by the first etchant at a second etch rate;

applying the first etchant to etch the contact layer to expose a portion of the Schottky layer; and

applying a second etchant to etch the portion of the Schottky layer exposed by the first etchant;

wherein second etch rate is substantially faster than the first etch rate when using the first etchant.

10. The method recited in claim 9 wherein the Schottky layer contains Aluminum.

11. The method recited in claim 10 wherein the Schottky layer comprises about 35 percent Aluminum.

12. The method recited in claim 11 wherein the contact layer is substantially free of Aluminum.

13. The method recited in claim 11 wherein the first etchant includes a carboxylic-acid based wet etchant.

14. The method recited in claim 13 wherein the first etchant is succinic acid.

15. The method recited in claim 11 wherein the second etchant is applied for a predetermined time.

~~16. A transistor structure comprising:~~

a source electrode;

a drain electrode;

a doped cap layer of $Ga_xIn_{1-x}As$ disposed below and in ohmic contact with the source electrode and the drain electrode and providing a cap layer opening;

an undoped resistive layer of $Ga_xIn_{1-x}As$ disposed below the cap layer and providing a resistive layer opening in registration with the cap layer opening and having a first width;

a Schottky layer of $Al_yIn_{1-y}As$ disposed below the

resistive layer;

an undoped channel layer disposed below the Schottky layer; and

a semi-insulating substrate disposed below the channel layer;

wherein a top surface of the Schottky layer beneath the resistive layer opening provides a recess having a second width smaller than the first width; and

wherein a gate electrode is in contact with a bottom surface of the recess provided by the Schottky layer.

17. The transistor recited in claim 16 wherein the ~~Schottky layer is doped~~.

18. A transistor, comprising:

a single crystal substrate having a lattice constant;

a channel layer disposed over the substrate, the channel layer having a lattice constant different from the lattice constant of the substrate;

a Schottky layer disposed over the channel layer, the Schottky layer having a lattice constant different from the lattice constant of the substrate;

a resistive layer disposed over the Schottky layer; and

a contact layer disposed over the resistive layer, the contact layer having a first recess therein, such first recess having a bottom surface terminating in a top surface of the resistive layer;

a second recess having sidewalls in the

resistive layer and the Schottky layer, such second recess having a bottom surface terminating in the Schottky layer.

19. The transistor recited in claim 18 wherein the lattice constant of the Schottky layer and a thickness of the Schottky layer are selected to compensate for differences in strain between: (a) the channel layer and the substrate; and, (b) the Schottky layer and the substrate.

20. The transistor recited in claim 19 wherein the lattice constant of the Schottky layer is smaller than the lattice constant of the substrate and the lattice constant of the channel layer is larger than the lattice constant of the substrate.

21. The transistor recited in claim 20 wherein the lattice constant of the substrate is intermediate the lattice constant of the channel layer and the lattice constant of the Schottky layer, the difference in lattice constants resulting in a compressive strain on the channel layer and a tensile strain on the Schottky layer.

22. The transistor recited in claim 18 wherein the Schottky layer has an indium concentration and the indium concentration in the Schottky layer is lower than an indium concentration in the channel layer.

23. The transistor recited in claim 22 wherein the substrate comprises indium phosphide.

24. The transistor recited in claim 22 wherein the Schottky layer comprises approximately $Al_{0.60}In_{0.40}As$.

25. The transistor recited in claim 22 wherein the channel layer comprises approximately $Ga_{0.35}In_{0.65}As$.

26. The transistor recited in claim 23 wherein the Schottky layer comprises approximately $Al_{0.60}In_{0.40}As$ and the channel layer comprises approximately $Ga_{0.35}In_{0.65}As$.

27. A transistor, comprising;

a substrate having a lattice constant;

a channel layer disposed over the substrate, the channel layer having a lattice constant;

a Schottky layer disposed over the channel layer, the Schottky layer having a lattice constant;

a resistive layer disposed over the Schottky layer; and

a contact layer disposed over the resistive layer, the contact layer having a first recess therein, such first recess having a bottom surface terminating in a top surface of the resistive layer; and

a second recess having sidewalls in the resistive layer and the Schottky layer, such second recess having a bottom surface terminating in the Schottky layer;

wherein at least one of the channel and Schottky layers has an indium concentration such that at least one of the lattice constants of the channel layer and lattice constant of the Schottky layer is different from the lattice constant of the substrate and a difference between conduction

band levels of the channel and Schottky layers is larger than if the channel and Schottky layers had the same lattice constant as the substrate.

28. The transistor recited in claim 27 wherein the larger conduction band discontinuity occurs between the Schottky and channel layers.

29. The transistor recited in claim 27 wherein the Schottky layer comprises approximately $Al_{0.60}In_{0.40}As$ and the channel layer comprises approximately $Ga_{0.35}In_{0.65}As$.

30. The transistor recited in claim 25 wherein the channel layer has an indium concentration such that the channel layer can support larger currents than if the channel layer and the substrate had the same lattice constant.

31. A transistor, comprising:

a semi-insulating indium phosphide substrate;

a channel layer of $Ga_xIn_{1-x}As$ disposed over the substrate layer;

a Schottky layer of $Al_yIn_{1-y}As$ disposed over the channel layer;

a resistive layer disposed over the Schottky layer;

a contact layer disposed over the resistive layer, the contact layer having a first recess, and the resistive layer and the Schottky layer having a second recess;

a source electrode in ohmic contact with the contact layer;

a drain electrode in ohmic contact with the contact layer; and

a gate electrode in Schottky contact with the Schottky layer.

32. The transistor recited in claim 31 further comprising a first doped layer, and a second doped layer.

33. The transistor recited in claim 32 further comprising a ratio of silicon doping concentration approximately 2.5 to 1.5 between the first doped layer and the second doped layer.

34. The transistor recited in claim 32 wherein the resistive layer further comprises approximately $Al_{0.48}In_{0.52}As$ and the contact layer further comprises approximately $Ga_{0.47}In_{0.53}As$.